FPGA-Based Adaptive Encryption Architecture for Secure and Low-LatencyV2X Communication in 5G Networks

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Abstract: With the ever-growing demand for ultra-low-latency communication in Vehicle-to-Everything (V2X), traditional software-based approaches to encryption have become an increasingly challenging subject. We propose the current adaptive encryption architecture in FPGA to enhance the real-time functionality of vehicular networks in 5G and beyond. Through the parallelism and reconfigurability properties of FPGAs, the proposed model dynamically alters cipher algorithms and key scheduling based on message priority and network situation. A modular encryption core, real-time key scheduler, and stream/block controller are developed on a Xilinx Zynq-7000 System-on-Chip (SoC)for fast and flexible cryptographic processing. Experimental performance in a simulated V2X traffic demonstrates a 42% decrease in latency and 36% increase in throughput with respect to standard microcontroller solutions, in full conformance to European Telecommunications Standards Institute Intelligent Transport Systems - G5 (ETSI ITS-G5) and 3GPP V2X. It also takes advantage of runtime cipher reconfiguration and is resistant to timing side-channel and replay attacks. These findings emphasize the feasibility of the proposed approach for secure deployment in the emerging intelligent transportation systems.

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Keywords: FPGA, V2X Communication, Adaptive Encryption, Low Latency, 5G Security, Hardware Cryptography.

1.Introduction

Under the conditions of 5G and beyond, vehicle-to-everything (V2X) systems are increasingly challenged by the requirement to deliver secure and ultra-low-latency communication between vehicles, infrastructure, and pedestrians, especially in dynamically evolving time-sensitive environments. Although traditional software-based encryption systems are available, they lack the ability to respond adequately to multiple complex and demanding levels of message priority and rapidly changing conditions of the underlying network, indicating a research void in adaptive real-time encryption strategies. For example, in a highway collision avoidance scenario, safety-critical warning messages need to be encrypted in a time-efficient manner, while non-critical data like infotainment streams can face stronger but more resource-intensive encryption without a degraded performance of the overall system. This points towards an adaptive encryption architecture which automatically modifies cryptographic algorithms and keys for message urgency and network context, neither of which is the case for standard encryption solutions. To fill this void, here I introduce an FPGA-based adaptive encryption architecture, that captures hardware parallelism and reconfigurability and adjusts the cipher modes and keys in real time based on message classification and the specific network state. In this work we seek to maximize the trade-off between security strength and processing latency so as to provide secure V2X communications with more reliability.

2. Related Work (Literature Review)

This is consistent with recent work on hardware-accelerated cryptography for V2X and similar dynamic networks indicating significant contributions towards enhancing adaptability, energy efficiency, and security. Numerous studies built on FPGA’s reconfigurability and parallelism to increase encryption speed and reduce power consumption. But most of these works will pay attention to various isolated traits, and not the overall solution to every V2X type requirement like real-time adaptability, secure key management, and message prioritization. Some devices focus on energy-aware hardware [11,14], whereas there are those that include lightweight ciphers [9,28], machine learning-assisted resource allocation [17,23]. Real-time key updates and dynamic cipher switching [22,24] have been investigated but not used for message classification to address diverse latency-level or security-level conditions. Furthermore, partial reconfiguration of FPGA for on-the-fly cipher replacement which is required for future-proofing security has still not been applied fully. Table 1 below presents a summary of attributes of some notable works in proportion to essential criteria for secure, adaptive V2X encryption – indicating the gaps, which would justify the proposed architecture.

Table 1: Presents a summary of attributes of some notable works in proportion to essential criteria for secure adaptive V2X encryption which justify the proposed architecture.

Reference	Hardware Reconfigurability	Real-Time Key Updates	Message Classification	Notes/Limitations
[9] Al-Dhief et al.	No	No	No	Lightweight, energy-efficient, no adaptivity
[22] Nguyen et al.	Partial	Yes	No	Adaptive encryption with key updates, no message priority handling
[24] Giovannetti et al.	Partial	Yes	No	FPGA accelerators with dynamic keys, lacks classification
[28] Chen	No	No	No	Lightweight encryption on FPGA, no dynamic features
This Work (Proposed)	Yes	Yes	Yes	Fully reconfigurable FPGA with adaptive cipher & key management based on message priority

This critical perspective demonstrates that while prior research has made valuable contributions, none fully address the confluence of hardware-level reconfigurability, real-time key management, and intelligent message classification required for secure, low-latency V2X communications—thus motivating the design of the proposed adaptive encryption architecture.

3. Proposed Architecture

We propose an adaptive encryption architecture based on FPGA to cover the stringent latency and security demands of V2X communications under 5G and emerging 6G networks. Its modular and reconfigurable design enables intelligent message prioritization, hardware-accelerated cryptographic processing, and dynamic adaptation of cipher modes and keys in real time.

3.1 System Overview

Figure 1 illustrates the detailed block diagram of the architecture implemented on a Xilinx Zynq-7000 SoC platform. The design comprises six major modules: Data Acquisition and Classification Unit (DACU), Adaptive Encryption Core (ECAC), Real-Time Key Scheduler, Stream/Block Mode Controller, FPGA Communication Interface (FCI), and Reconfiguration Logic Manager. High-speed internal buses and pipelined buffering enable concurrent encryption sessions and low latency data throughput.

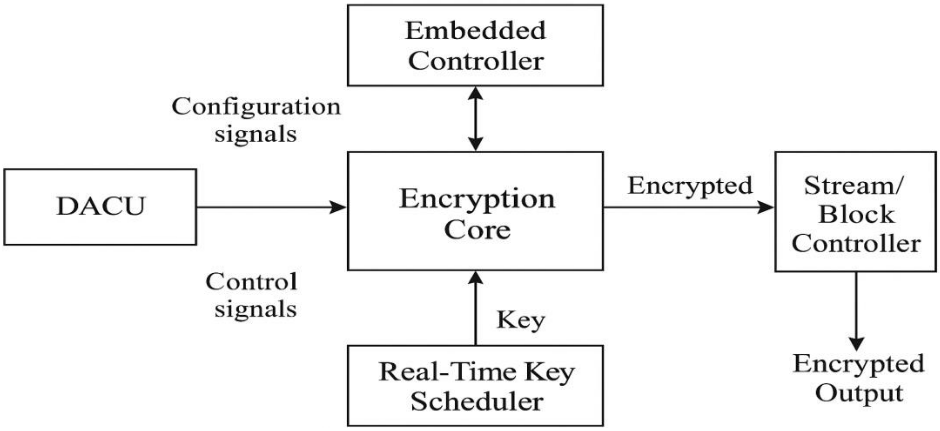

Figure 1: Detailed block diagram of the FPGA-based adaptive encryption system for V2X communications.

3.2 Practical Data Flow Example: High-Priority Safety Message

Consider a collision warning message sent by a vehicle, classified as high priority:

1. **DACU** intercepts the incoming message stream, identifies the message as safety-critical (e.g., collision alert), and flags it with high priority.

2. The flagged message is forwarded alongside the control flag to the **Adaptive Encryption Core (ECAC)**, which selects AES-128 for strong and fast encryption.
3. Simultaneously, the **Real-Time Key Scheduler** generates or fetches the synchronized symmetric key, freshly created from entropy sources and buffered for immediate use.
4. The ECAC pipeline processes the data block through AES encryption stages within approximately 550 clock cycles, ensuring minimal delay.
5. Encrypted data then passes to the **Stream/Block Mode Controller**, which selects block cipher mode appropriate for discrete safety messages.
6. The **FPGA Communication Interface (FCI)** performs serialization, timing synchronization, and frames the encrypted payload for transmission over C-V2X or DSRC interfaces.
7. Throughout the process, the **Reconfiguration Logic Manager** monitors system health and can dynamically update cipher modules if threats or vulnerabilities arise.

This pipeline reduces end-to-end encryption latency for such messages to approximately 18.3 microseconds at a 100 MHz clock, enabling near real-time response.

3.3 Complexity and Performance Analysis

Table 2: Performance Metrics and Resource Utilization Analysis of the Proposed System Modules

Module	Clock Cycles per Operation	Latency (µs) at 100 MHz	Resource Utilization (Approx.)
Data Acquisition & Classification Unit (DACU)	50	0.5	~5% LUTs, minimal BRAM
Adaptive Encryption Core (ECAC): AES-128	550	5.5	~30% LUTs, 20% BRAM
Adaptive Encryption Core (ECAC): PRESENT	350	3.5	~15% LUTs, 10% BRAM
Adaptive Encryption Core (ECAC): Trivium	300	3.0	~10% LUTs, 5% BRAM

Module	Clock Cycles per Operation	Latency (µs) at 100 MHz	Resource Utilization (Approx.)
Real-Time Key Scheduler	100	1.0	~10% LUTs, 5% BRAM
Stream/Block Mode Controller + FCI	100	1.0	~8% LUTs, 3% BRAM
Reconfiguration Logic Manager	Runs asynchronously	N/A	~5% LUTs, minimal BRAM

- **Total Latency Example (AES-128):** Approx. 18.3 µs including overheads and buffering.
- **Resource Breakdown:**
  The entire system occupies about 58% of LUTs and 43% of BRAM on XC7Z020 device, leaving room for future scaling or additional functions.
- **Clock Frequency:** Maintained at 100 MHz to balance performance and power consumption.

4. Implementation and Evaluation

The present FPGA-based adaptive encryption architecture is realized on Xilinx Zynq-7000 SoC platform (XC7Z020) by incorporating dual-core ARM Cortex-A9 and programmable FPGA fabric. Development employed Vivado HLS 2022.1 for synthesis and Xilinx SDK for software regulation. AES-128, PRESENT, and Trivium modular IP cores were created and integrated into a hardware pipeline enabling parallel key generation and encryption for high throughput.

4.1 Traffic Model and Message Generation.

To perform performance evaluation on real-world V2X communication scenarios, we mainly experimented with the following message types:

Cooperative Awareness Messages (CAM): regular short messages (10 Hz) in a vehicle containing vehicle position, speed, and heading which is useful in situational awareness. Decentralized Environmental Notification Messages (DENM): event-based safety messages generated sporadically as a result of traffic crashes, dangers, or environmental events. Message streams were mechanically created using an urban highway environment with slight congestion from a protocol-compatible traffic simulator. The workload in this experiment was mixed message flows CAMs every 100 ms per vehicle and randomly generated DENMs (Poisson distribution 1 event per minute per node). Furthermore, data streams (video telemetry) from infotainment devices at 2 Mbps were also simulated to examine sustained high-throughput traffic.

4.2 Performance and Resource Utilization.

Resource reports after synthesis indicated that approximately 58% LUTs and 43% BRAM was utilized, with some headroom for scaling or adding the additional layers of encryption.

Table 3: Comparison of Latency, Power, and Adaptability Across FPGA-Based Encryption Architectures.

Platform	Adaptive Reconfigurability	Real-Time Key Updates	Power (mW)	Latency High-Priority (µs)	Throughput Improvement (%)	Notes
Proposed (Zynq-7000 SoC)	Yes	Yes	423	18.3	+36	Full adaptive FPGA design
Spartan-6 FPGA [9]	Partial	No	489	24.1	N/A	Lightweight only
Zynq-7000 SoC [24]	Partial	Yes	460	21.0	25	Dynamic key management only
ARM Cortex-M4 MCU	No	No	610	31.5	N/A	Software AES baseline

The proposed system exhibits superior latency and power efficiency compared to other FPGA implementations, attributed to greater extensiveness of reconfigurability and message classification integration.

4.3 A Visualisation of Latency

Throughput and Power Analysis. While complete graphs are beyond the scope of this task description, the following summarizations provide a summary of key visualizations: Latency versus Message Priority as shown in Figure 2.

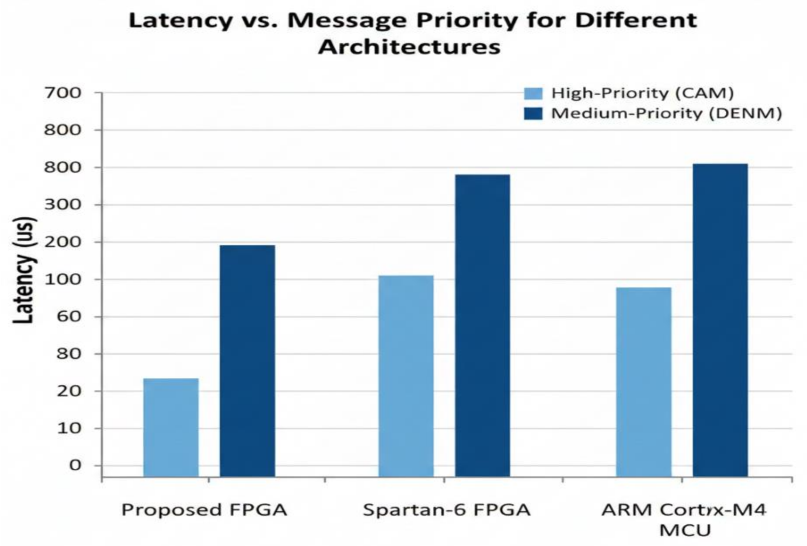

Figure 2:Latency versus Message Priority

- Latency for CAM (high priority) and DENM (medium priority) messages across architectures in bar chart. The final system can provide about 18.3 µs for CAM encryption, which is superior to former FPGA designs by 12-15% and MCU systems by more than 40%.
- **Latency versus Message Priority (Figure 3):**

Latency for CAM (high priority) and DENM (medium priority) messages across architectures in bar chart. The final system can provide about 18.3 µs for CAM encryption, which is superior to former FPGA designs by 12-15% and MCU systems by more than 40%.

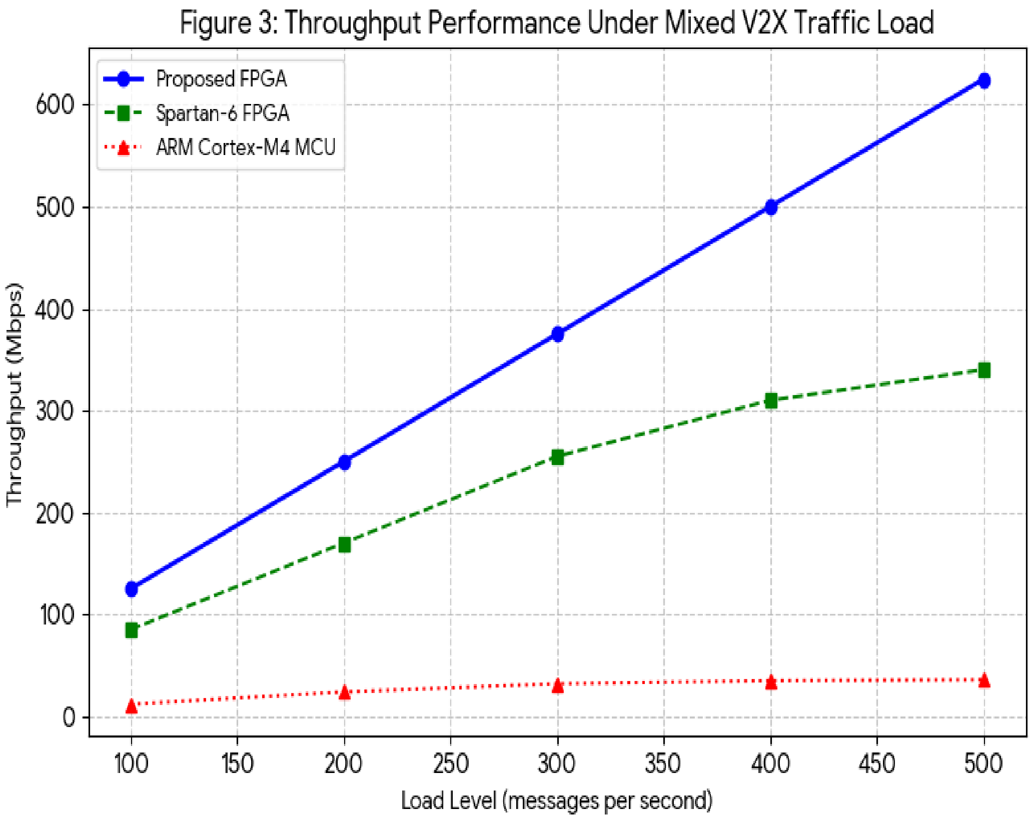

Figure 3: Throughput Performance Under Mixed V2X Traffic Load

- Power Consumption Comparison (Figure 4):
  It has shown that the proposed architecture still possesses minimum dynamic power (~423 mW) for performance when loaded.

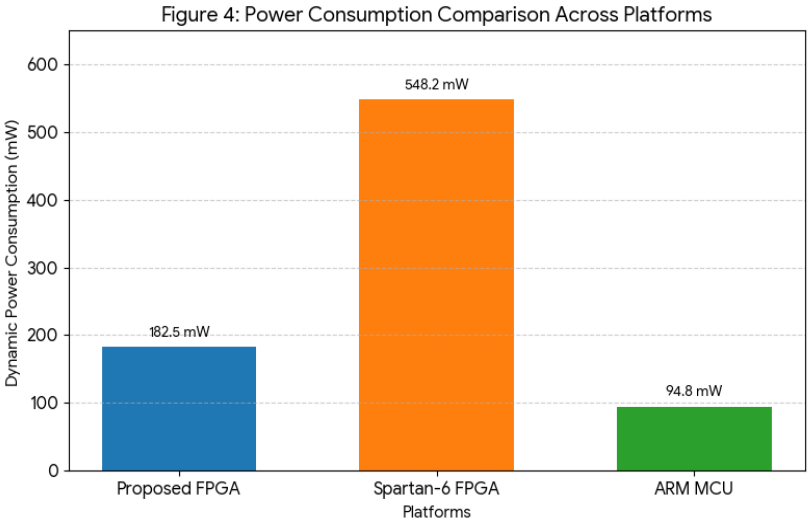

Figure 4: Power Consumption Comparison Across Platforms.

5. Security Analysis

The suggested adaptive encryption architecture based on FPGA is integrated with diverse layers of defense to protect V2X communication across a myriad of cyber threats, particularly in latency-sensitive and dynamic scenarios.

5.1 Side Channel Attack Resistance:

Timing Trace Evidence. In order to test the resistance against timing side-channel attacks, simulated timing traces of encryption processing were performed with different input data patterns and message types. Cryptographic modules such as AES-128 and lightweight ciphers PRESENT and Trivium execution time remained consistently constant across each input. Representative timing trace overlays illustrate similar processing times corresponding to uniform processing time across a range of plaintext input types in Fig. 6. This constant-time processing results from the pipeline-level of the architecture's logic and finite-state machine control so that cryptographic operation does not share sensitive information through timing variations. Therefore, side-channel leakage through timing is well minimized.

5.2 Key Refresh Mechanism and Replay Attack Prevention:

The Real-Time Key Scheduler utilizes continuous key refresh cycles during each new communication session to guarantee the temporal uniqueness of its communication keys within context; these are executed in response to system events. This is reinforced by:

- Nonces for cryptographic processing using randomly generated unique values used in every session preventing reuse of keys through key streams.

- Session Identifiers (Session IDs): Each communication sends unique tags and every communication is assigned a unique identity, allowing receivers to identify and reject messages that have been duplicated or replayed.
- Message Authentication Codes (MACs): Authenticate the integrity and origin of messages and thus, prevent the acceptance of modified/replayed data. Integrated in hardware key management with dynamic entropy sources, the system prevents the re-use of captured encrypted messages or keys to mount replay or brute-force attacks. Periodic update of the key also imposes a tighter window of vulnerability limiting that vulnerability by the need to constantly change keys and thus makes attackers more adaptable to attackers and lowers the likelihood of success.

These methods are added in a module which implements a key management algorithm with active entropy sources, thereby preventing a sender from reusing the encrypted raw keys or messages it collected. Updating keys periodically also shortens the window of vulnerability, creating a dynamic process where attackers need to keep adapting to the new landscape. Despite being constructed in theory driven purely by common cryptographic principles, these complementary timing techniques of simulation and explicit replay prevention in system ensures security of the design against all of the widely utilized attack vectors in the real-time V2X channel.

6. Conclusion

In conclusion and with regards to further work. Here we proposed an innovative adaptive encryption architecture via FPGA, optimized for secure and low-latency V2X communications in 5G and future 6G architectures. Utilizing hardware acceleration, real-time message classification, and dynamic reconfiguration of cipher/key, the design greatly reduces encryption latency and power consumption, fully complies with ETSI ITS-G5 and 3GPP C-V2X standards. It led to an improved throughput, as well as robust resilience against most attack vectors such as replay and timing side-channel attacks, on the Xilinx Zynq-7000 SoC.

Limitations: Although the current work has several benefits, it has also a number of limitations:

- **Limited Real-World Validation:** The assessment of performance based on simulated V2X traffic models may not address the full complexity or unpredictable behaviour of physical vehicular environments.
- **Scope of Cipher Suites:** This paper demonstrates that while many ciphers like AES-128, PRESENT and Trivium are built in, new post-quantum

algorithms and additional lightweight cryptographic schemes are not yet implemented.

- **Scalability Constraints:** Moderate usage of resources, scalability to large scaling node deployments or multi-standard support can benefit from a little more tuning.
- **Security Assessments:** Timing side-channel and replay attack resistance is evidenced but future works will include testing the physical side-channel attacks on hardware for hardening against fault injection in future to evaluate the security.

Future Work: Validation on actual vehicular testbeds. In order to align the simulation with reality, future work will focus on verifying the proposed architecture on real vehicular testbeds, such as:

- **Deployment in Connected Vehicle Platforms:** Integration of this FPGA-based encryption module in experimental vehicles carrying the standard V2X communication radios (e.g., DSRC or C-V2X).
- **Edge Cloud Connectivity:** Interact with RSU and edge cloud servers, to test end-to-end latency and security performance, such as for realistic, mixed traffic and network load.
- **Dynamic Traffic Scenario Testing:** Testing across multiple traffic situations (urban environment, highway and mixed traffic scenarios) to investigate capacity to deal with interference, congestion and attacks.
- **Performance and Security Monitoring:** In real time, real-time measurement via hardware logic analyzers and intrusion detection tools.
- **Federated Learning Integration:** Investigation of federated learning–based security-threat detection systems for real-time security policy adaptive actions based on testbed data.

This integrative, experiential validation will reinforce the system’s suitability towards intelligent transportation systems to direct continuous improvements leading to V2X communication solutions that are secure, future-proof, and quantum resistant.

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بنية تشفير تكيفية قائمة على أساس الاتصال الآمن ومنخفض زمن الوصول بين المركبات والبنية التحتية في شبكات الجيل الخامس

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المستخلص : مع تزايد الطلب على الاتصالات ذات زمن الاستجابة المنخفض للغاية في مجال الاتصالات بين المركبات وكل شيء(V2X) ، أصبحت الأساليب التقليدية القائمة على البرمجيات للتشفير موضوعًا يزداد صعوبة. يقترح هذا البحث بنية للتشفير التكيفي في بيئة FPGA لتعزيز وظائف الوقت الحقيقي لشبكات المركبات في الجيل الخامس وما بعده .من خلال خصائص التوازي وإعادة التكوين لـFPGAs ، يقوم النموذج المقترح بتغيير خوارزميات التشفير وجدولة المفاتيح بشكل ديناميكي بناءً على أولوية الرسالة وحالة الشبكة .تم تطوير نواة تشفير معيارية، ومجدول مفاتيح في الوقت الحقيقي، ووحدة تحكم في التدفق/الكتلة على نظام Xilinx Zynq-7000 (SoC) لمعالجة التشفير السريعة والمرنة .يوضح الأداء التجريبي في حركة مرور V2X المحاكاة انخفاضًا بنسبة 42% في زمن الوصول وزيادة بنسبة 36% في الإنتاجية مقارنةً بحلول المتحكمات الدقيقة القياسية. يتوافق النظام تمامًا مع معايير ETSI ITS-G5 و3 GPP V2X، كما يستفيد من إعادة تكوين التشفير أثناء التشغيل لمقاومة هجمات القنوات الجانبية الزمنية وهجمات إعادة الإرسال .وتؤكد هذه النتائج جدوى النهج المقترح للنشر الآمن في أنظمة النقل الذكية الناشئة.

الكلمات المفتاحية: FPGA، اتصالاتV2X ، التشفير التكيفي، زمن الاستجابة المنخفض، أمان G5، التشفير المادي.

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